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EXAMINER	
TRAN, DENISE	

ART UNIT	PAPER NUMBER
2186	6

DATE MAILED: 04/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/643,636	KRANTZ ET AL.	
	Examiner	Art Unit	
	Denise Tran	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-17,22 and 24-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *29* is/are allowed.

6)☒ Claim(s) *1-7,9-17,22 and 24-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The applicant's amendment filed 2/9/04 has been considered. Claims 1-7, 9-17, 22, and 24-29 are presented for examination. Claims 8, 18-21, and 23 have been canceled.

2. The objection to the abstract of the disclosure is **withdrawn** due to the applicant's amendment filed 2/9/04.

3. The 112 rejections with respect to claims 28-29 are **withdrawn** due to the applicant's amendment filed 2/9/04.

4. Claim 29 is allowable over the prior art of record.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3, 5, 9-11, 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Proch et al., U. S. Patent No. 6,381,659 (hereinafter Proch) in view of Holmes, U.S. Patent No. 6,490,635 .

As per claims 1, Proch shows a buffer memory controller for a disk controller (e.g., fig. 2, el. 140) the buffer memory controller comprising:

A data buffer (e.g., fig. 2, fig. 2, buffer 144) configured to buffer write operation data between a buffer memory (e.g., fig. 2, buffer 25) and a write head of a disk (e.g., fig. 2, els 31-32);

A plurality of address registers configured to store, for each of a plurality of write operations, an address identifying a location of corresponding write operation data stored within the buffer memory (e.g., fig. 2, els. 152a-b, 154a-b, 148); and

Controller logic configured to transfer, for each of the write operations, the corresponding write operation data from the buffer memory to the data buffer based at least upon the corresponding address stored in the address registers (e.g., col. 6, lines 30-65) and the controller logic is further configured to transfer the data of at least two operations based upon a single command to the buffer memory controller (e.g., col. 10 , lines 60). Proch does not explicitly show the use of a hard disk or a hard disk controller and writing the data in an order other than the order in which the write operations were received. Holmes shows the concept and the advantages of providing a hard disk or a hard disk controller (e.g., col. 1, line 15) are well known and expected in the art and writing the data in an order other than the order in which the write operations were received (e.g. col. 1, lines 15-25 and lines 40-60, col. 2, lines 19-20 and col. 5, lines 61-64). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a hard disk or a hard disk controller because it would

allow more data to be stored and accessed more quickly and enhance disk drive performance.

As per claims 2-3 and 25-27, Proch shows a plurality of blocks count registers configured to stored, for each of the write operations, the corresponding amount of write operation data stored within the buffer memory (e.g., col. 8, lines 25-45); wherein the controller logic is configured to perform the transfers based additionally upon the quantities stored in the block count registers (e.g., col. 9, lines 25-45); and Proch teaches for each of write operations, loading a different one of a plurality of block count registers of the buffer memory controller with a value specifying an amount of write operation data associated with the respective write operation (e.g., col. 7, lines 40-55; col. 8, lines 25-45); wherein the address registers and the block count registers are load with the addresses and amounts of the data of the write operations in the order in which the write operations are to be executed (e.g., col. 7, lines 40-55; col. 8, lines 25-45).

As per claims 5, 9-11 Proch shows the data buffer operated as a FIFO (e.g., fig. 2, FIFO 144); the controller logic is further configured to transfer the data of at least two operations based upon a single command to the buffer memory controller (e.g., col. 10 , lines 60); a busy flag to indicate whether the address registers are full (e.g., fig. 3b, FIFO full); the number of address registers is at least 4, (e.g., fig. 2, els. 152a-b and 154a-b) or at least 8 (e.g., col. 11, lines 15-20).

As per claim 24, Proch shows the use of a buffer memory controller of a hard disk controller, comprising:

For each of a plurality of write operations, receiving in a different one of a plurality of address registers of the buffer memory controller, an address, within a buffer memory, of write operation data of the respective write operation(e.g., col. 6, lines 50-65 and col. 10, line 45 to col. 11, line 15);

Receiving a single command to provide the write operation data of the plurality of write operations (e.g., col. 10 , lines 60); and

Writing the data of the plurality of write operations (e.g. col. 10, line 60 to col. 11, line 35). Proch does not specifically show the use of writing in an order other than the order in which the data was received in the buffer memory. Holmes shows the use of writing the data of the second write operation prior to writing the data of the first write operation (e.g. col. 1, lines 15-25 and lines 40-60, col. 2, lines 19-20 and col. 5, lines 61-64). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a hard disk or a hard disk controller because it would allow more data to be stored and accessed more quickly and. enhance disk drive performance.

As per claim 28, Proch shows a disk drive controller comprising:

a buffer memory for storing write operation data (e.g., fig. 2, el. 25);

a buffer memory controller comprising:

A data buffer (e.g., fig. 2, fig. 2, buffer 144) configured to buffer write operation data between a buffer memory (e.g., fig. 2, buffer 25) and a write head of a disk (e.g., fig. 2, els 31-32);

A plurality of address registers configured to store, for each of a plurality of write operations, an address identifying a location of corresponding write operation data stored within the buffer memory (e.g., fig. 2, els. 152a-b, 154a-b, 148); and

Controller logic configured to transfer, for each of the write operations, the corresponding write operation data from the buffer memory to the data buffer based at least upon the corresponding address stored in the address registers (e.g., col. 6, lines 30-65). Proch does not explicitly show firmware code that is executed by a microprocessor, the firmware code configured to enable the microprocessor perform write operations in an order other than the other in which the write operations are received by the controller. Holmes firmware code that is executed by a microprocessor, the firmware code configured to enable the microprocessor perform write operations in an order other than the other in which the write operations are received by the controller (e.g., col. 1, lines 20-25 and lines 35-60; and col. 5, lines 60-64. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching Holmes into the system of Proch because it would allow enhance disk drive performance.

7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Holmes, U.S. Patent No. 6,490,635 in view of Proch et al., U. S. Patent No. 6,381,659

(hereinafter Proch) or Applicant's admitted prior art, Applicant's specification pages 1-2 (hereinafter AAPA) and in further view of Official Notice.

As per claim 12, Holmes teaches a method of operating a hard disk unit, the method comprising:

(A) receiving a first write operation (e.g., col. 2, lines 19-20);

(B) subsequent to (A), receiving a second write operation (e.g., col. 2, lines 19-20);

(C) writing the data of the second write operation to a disk (e.g., col. 1, lines 15-25 and lines 40-60; and col. 5, lines 61-64).

Holmes does not specifically show the use of receiving a single command from a processor to provide the data from the first write operation and the data from the second write operation to a disk formatter. Proch or AAPA shows the use of a single command to transfer to a disk formatter the data of multiple write operations (e.g. Proch, col. 10, lines 60 to col. 11, lines 30 and AAPA, page 1, line 29 to page 2, line 5, respectively). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Proch or AAPA to Holmes because it would provide for faster access to data on the disk and enhance disk drive performance. "Official Notice" is taken that both the concept and the advantages of providing a disk formatter are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide for a disk formatter because it would allow address or block count to be access in the same order as received and data to be processed in a predetermined format.

8. Claims 4, 6-7, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Proch et al., U. S. Patent No. 6,381,659 (hereinafter Proch) in view of Holmes, U.S. Patent No. 6,490,635, and further in view of Official Notice.

As per claim 22, Proch shows a method of operating a disk controller , the method comprising:

Receiving a first write operation (e.g. col. 10, lines 47-67);

Receiving a second write operation subsequent to receiving the first write operation (e.g. col. 10, lines 47-67);

Loading a first address register of a buffer memory controller with an address in a buffer memory of write operation data of a first write operation (e.g., col. 6, lines 50-65); and

Loading a second address register of a buffer memory controller with an address in the buffer memory of write operation data of a second write operation (e.g., col. 6, lines 50-65);

Wherein the first address register is different than the second address register, wherein the first address register is different than the second address register, and wherein the first write operation is different than the second write operation (e.g., col. 10, line 45 to col. 11, line 15); or receiving a command to provide the write operation data of the plurality of write operations (e.g., col. 10 , lines 60) and receiving a single command from a processor to provide both the data of the first write operation and the

data of the second write operation (e.g., col. 10 , lines 60). Proch does not explicitly show the use of a hard disk or a hard disk controller, disk formatter and writing the data of the second write operation prior to writing the data of the first write operation. Holmes shows the concept and the advantages of providing a hard disk or a hard disk controller (e.g., col. 1, line 15) are well known and expected in the art and writing the data of the second write operation prior to writing the data of the first write operation (e.g. col. 1, lines 15-25 and lines 40-60, col. 2, lines 19-20 and col. 5, lines 61-64). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a hard disk or a hard disk controller because it would allow more data to be stored and accessed more quickly and enhance disk drive performance. "Official Notice" is taken that both the concept and the advantages of providing a disk formatter are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide for a disk formatter because it would allow address or block count to be access in the same order as received and data to be processed in a predetermined format.

As per claims 4 and 6-7, Proch does not explicitly show the block count registers operate as a FIFO, data register is configured to supply write operation data to a disk formatter; or the address registers operate as a FIFO. "Official Notice" is taken that both the concept and the advantages of providing a block count registers as FIFO, disk formatter, or address registers as FIFO are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide providing a block count registers as FIFO, providing data to a disk formatter,

or address registers as FIFO because it would allow address or block count to be access in the same order as received and data to be processed in a predetermined format.

9. Claims 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holmes, U.S. Patent No. 6,490,635 in view of Proch et al., U. S. Patent No. 6,381,659 (hereinafter Proch) or Applicant's admitted prior art, Applicant's specification pages 1-2 (hereinafter AAPA).

As per claim 24, Holmes shows the use of a buffer memory controller of a hard disk controller, comprising:

For each of a plurality of write operations, receiving in a different one of a plurality of address registers of the buffer memory controller, an address, within a buffer memory, of write operation data of the respective write operation (i.e., Ram , memory unit is a collection of storage registers; e.g., fig. 5, els. LBA and col. 3, lines 15-35; col. 5, lines 10-12);

(e.g., col. 10 , lines 60); and

Writing the data of the plurality of write operations in an order other than the order in which the data of each of plurality of write operations was received by the buffer memory (e.g. col. 1, lines 15-25 and lines 40-60, col. 2, lines 19-20 and col. 5, lines 61-64). Holmes does not specifically show the use receiving a single command to provide the write operation data of the plurality of write operations. Proch and AAPA show the use of receiving a single command to provide the write operation data of the plurality of

write operations (e.g. col. 10, lines 60 to col. 11, lines 30 and page 1, line 29 to page 2, line 5, respectively). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Proch or AAPA to Holmes because it would provide for faster access to data on the disk and enhance disk drive performance.

As per claims 25-27, Holmes teaches for each of write operations, loading a different one of a plurality of block count registers of the buffer memory controller with a value specifying an amount of write operation data associated with the respective write operation (i.e., Ram , memory unit is a collection of storage registers; e.g., fig. 5, els. block count 540 and col. 3, lines 15-35); wherein the address registers and the block count registers are load with the addresses and amounts of the data of the write operations in the order in which the write operations are to be executed (e.g., col. 5, lines 63-67); for one of the write operations, transferring write operation data from the buffer memory, the amount of which write operation data is specified by the value in the corresponding block count register and the address of which write operation data is specified by the address corresponding address register (e.g., col. 3, lines 15-35); repeating (D) for each of the remaining write operations (e.g., col. 3, lines 15-35).

10. Claims 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holmes, U.S. Patent No. 6,490,635 in view of Proch et al., U. S. Patent No. 6,381,659 (hereinafter Proch) or Applicant's admitted prior art, Applicant's specification pages 1-2

(hereinafter AAPA) and in further view of Official Notice and further view of in view of Au, U.S. Patent No. 5,729,718.

As per claims 13-17, Holmes does not explicitly show the use of determining that the first write operation and the second write operation write data to the same track; determining that second write operation has a lower ending sector number than the starting sector number of the first write operation; determining that second write operation is located before the first write operation relative to the position where the write head of the disk is capable of first writing to the track; wherein a portion of the data of the first write operation and a portion of the data of the second write operation are written to the disk during a single revolution; wherein a portion of the data of the first write operation and the data of the second write operation are written to the disk during a single revolution. Au shows determining that the first write operation and the second write operation write data to the same track (e.g., col. 4, lines 35-40); determining that second write operation has a lower ending sector number than the starting sector number of the first write operation (e.g., (e.g., col. 3, 50-55); determining that second write operation is located before the first write operation relative to the position where the write head of the disk is capable of first writing to the track; wherein a portion of the data of the first write operation and a portion of the data of the second write operation are written to the disk during a single revolution; wherein a portion of the data of the first write operation and the data of the second write operation are written to the disk during a single revolution. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Au to the system of Holmes

because it would allow improve data throughput of a storage device by reordering commands to minimize latency including both seeking time and rotational latency.

As per claims 14-17, Holmes shows determining that second write operation has a lower ending sector number than the starting sector number of the first write operation (e.g., col. 6, lines 45-65; col. 6, lines 25-30; col. 5, lines 40-55); determining that second write operation is located before the first write operation relative to the position where the write head of the disk is capable of first writing to the track (e.g., col. 6, lines 25-30; col. 5, lines 40-55); wherein a portion of the data of the first write operation and a portion of the data of the second write operation are written to the disk during a single revolution (col. 4, lines 35-58); wherein a portion of the data of the first write operation and the data of the second write operation are written to the disk during a single revolution (col. 4, lines 35-65).

11. Applicants remarks filed 2/9/04 have been considered but are not persuasive.

12. In the remarks, Applicants argued in substance that (1) Holmes does not teach or suggest the method as recited in amended claim 12. In particular, Holmes does not appear to teach receiving a single command to transfer to a disk formatter the data of multiple write operations, wherein the data is written in an order other than the order in which the data was received by the hard disk unit.

As to point (1) the limitation "a single command to transfer to a disk formatter the data of multiple write operations" is a new issue for claim 12. Therefore, as shown

above both Proch and AAPA show the use of a single command to transfer to a disk formatter the data of multiple write operations (e.g. col. 10, lines 60 to col. 11, lines 30 and page 1, line 29 to page 2, line 5, respectively). As per the limitation "the data is written in an order other than the order in which the data was received by the hard disk unit", Holmes clearly shows this limitation (e.g. col. 1, lines 15-25 and lines 40-60, col. 2, lines 19-20 and col. 5, lines 61-64).

13. In the remarks, Applicants argued in substance that (2) Holmes does not appear to teach a method for writing the data to a disk.

As to point (2) the examiner disagrees because Holmes is clearly directed to optimizing disk accesses (i.e., reading and writing) (e.g. col. 1, lines 36-62).

14. In the remarks, Applicants argued in substance that (3) neither Proch nor Holmes nor a combination of Proch and Holmes teaches or suggests a buffer memory controller as recited in claim 1. In particular, neither reference teaches a buffer memory controller having controller logic configured to, in response to a single command, transfer data from a plurality of write operations, wherein the data is transferred in an order other than the order in which the data was received by the buffer memory.

As to point (3) the examiner disagrees for similar reasons as stated in the examiner's response (1). Specifically, Proch shows the use of a buffer memory controller having controller logic configured to, in response to a single command, transfer data from a plurality of write operations (e.g. col. 10, lines 60 to col. 11, lines

30). AAPA also shows the use of in response to a single command, transfer data from a plurality of write operations (page 1, line 29 to page 2, line 5). Furthermore, Holmes shows the use of the data is transferred in an order other than the order in which the data was received by the buffer memory (e.g. col. 1, lines 15-25 and lines 40-60, col. 2, lines 19-20 and col. 5, lines 61-64).

15. In the remarks, Applicants argued in substance that (4) Holmes does not appear to disclose the use of a plurality of address registers, as recited in claim 1, to store addresses of data stored within a buffer memory.

As to point (4) Holmes was not relied upon to show the above limitation, Proch was. Proch shows the use of a plurality of address registers configured to store, for each of a plurality of write operations, an address identifying a location of corresponding write operation data stored within the buffer memory (e.g., fig. 2, els. 152a-b, 154a-b, 148).

16. In the remarks, Applicants argued in substance that (5) the cited references do not teach or suggest the recited combination of limitations in claim 22.

As to point (5) the examiner disagrees because Proch shows a method of operating a disk controller , the method comprising:

Receiving a first write operation (e.g. col. 10, lines 47-67);

Receiving a second write operation subsequent to receiving the first write operation (e.g. col. 10, lines 47-67);

Loading a first address register of a buffer memory controller with an address in a buffer memory of write operation data of a first write operation (e.g., col. 6, lines 50-65); and

Loading a second address register of a buffer memory controller with an address in the buffer memory of write operation data of a second write operation (e.g., col. 6, lines 50-65);

Wherein the first address register is different than the second address register, wherein the first address register is different than the second address register, and wherein the first write operation is different than the second write operation (e.g., col. 10, line 45 to col. 11, line 15); or receiving a command to provide the write operation data of the plurality of write operations (e.g., col. 10 , lines 60) and receiving a single command from a processor to provide both the data of the first write operation and the data of the second write operation (e.g., col. 10 , lines 60). Proch does not explicitly show the use of a hard disk or a hard disk controller, disk formatter and writing the data of the second write operation prior to writing the data of the first write operation. Holmes shows the concept and the advantages of providing a hard disk or a hard disk controller (e.g., col. 1, line 15) are well known and expected in the art and writing the data of the second write operation prior to writing the data of the first write operation (e.g. col. 1, lines 15-25 and lines 40-60, col. 2, lines 19-20 and col. 5, lines 61-64). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a hard disk or a hard disk controller because it would allow more data to be stored and accessed more quickly and enhance disk drive performance. "Official

Notice" is taken that both the concept and the advantages of providing a disk formatter are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide for a disk formatter because it would allow address or block count to be access in the same order as received and data to be processed in a predetermined format.

17. In the remarks, Applicants argued in substance that (6) the cited references do not teach or suggest the recited combination of limitations in claim 28.

As to point (6) the examiner disagrees because Proch shows a disk drive controller comprising:

a buffer memory for storing write operation data (e.g., fig. 2, el. 25);

a buffer memory controller comprising:

A data buffer (e.g., fig. 2, fig. 2, buffer 144) configured to buffer write operation data between a buffer memory (e.g., fig. 2, buffer 25) and a write head of a disk (e.g., fig. 2, els 31-32);

A plurality of address registers configured to store, for each of a plurality of write operations, an address identifying a location of corresponding write operation data stored within the buffer memory (e.g., fig. 2, els. 152a-b, 154a-b, 148); and

Controller logic configured to transfer, for each of the write operations, the corresponding write operation data from the buffer memory to the data buffer based at least upon the corresponding address stored in the address registers (e.g., col. 6, lines 30-65). Proch does not explicitly show firmware code that is executed by a

microprocessor, the firmware code configured to enable the microprocessor perform write operations in an order other than the other in which the write operations are received by the controller. Holmes firmware code that is executed by a microprocessor, the firmware code configured to enable the microprocessor perform write operations in an order other than the other in which the write operations are received by the controller (e.g., col. 1, lines 20-25 and lines 35-60; and col. 5, lines 60-64. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching Holmes into the system of Proch because it would allow enhance disk drive performance.

18. Applicant has failed to seasonably challenge the examiner's Official Notices in the previous office action, those limitations are now considered as prior art. MPEP 2144.03.

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (703) 305-9823. The examiner can normally be reached on Monday, Thursday and an alternated Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for central Official communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

D.T.
April 18, 2004